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BoogarLists | Directory of Semiconductor Equipment Wafer-Level Testing and Test During Burn-In for Integrated Circuits BoogarLists | Directory of Semiconductor Manufacturers Semiconductor International Plunkett's Infotech Industry Almanac 2006 State-of-the-Art Program on Compound Semiconductors : (SOTAPOCS XLII) and Processes at the Compound-Semiconductor/Solution Interface An Engineer's Guide to Automated Testing of High-speed Interfaces Private Equity in Action IEEE/CPMT International Electronics Manufacturing Technology Symposium Testing of Interposer-Based 2.5D Integrated Circuits IEEE/CPMT International Electronic Manufacturing Technology Symposium : [proceedings]. Advanced Packaging BoogarLists | Directory of Fabless Manufacturing Test and Diagnosis of Analogue, Mixed-signal and RF Integrated Circuits BoogarLists | Directory of Electronics Systems Design SEOUL Magazine(?? ???) May 2018 ESD Basics Electronic Devices Multiple Choice Questions and Answers (MCQs) Security in Computing and Communications Silicon Germanium Materials and Devices - A Market and Technology Overview to 2006 Dictionary of Occupational Titles Area Array Interconnection Handbook NASA Tech Briefs Semiconductor Memories Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Signal Integrity Characterization Techniques Power-Aware Testing and Test Strategies for Low Power Devices BoogarLists | Directory of Communications Technologies WiMAX Monthly Newsletter June 2010 Official Gazette of the United States Patent and Trademark Office Advanced Test Methods for SRAMs Design to Test Standard & Poor's Stock Reports Dielectrics in Emerging Technologies Cleaning Technology in Semiconductor Device Manufacturing Advanced Packaging Wafer-Level Testing and Test Planning for Integrated Circuits Engineering Horizons Trace Analysis of Semiconductor Materials Multi-run Memory Tests for Pattern Sensitive Faults

Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions. This book is the second edition of Design to Test. The first edition, written by myself and H. Frank Binnendyk and first published in 1982, has undergone several printings and become a standard in many companies, even in some countries. Both Frank and I are very proud of the success that our customers have had in utilizing the information, all of it still applicable to today's electronic designs. But six years is a long time in any technology field. I therefore felt it was time to write a new edition. This new edition, while retaining the basic testability prin ciples first documented six years ago, contains the latest material on state-of-the-art testability techniques for electronic devices, boards, and systems and has been completely rewritten and up dated. Chapter 15 from the first edition has been converted to an appendix. Chapter 6 has been expanded to cover the latest tech nology devices. Chapter 1 has been revised, and several examples throughout the book have been revised and updated. But some times the more things change, the more they stay the same. All of the guidelines and information presented in this book deal with the three basic testability principles-partitioning, control, and visibility. They have not changed in years. But many people have gotten smarter about how to implement those three basic test ability principles, and it is the aim of this text to enlighten the reader regarding those new (and old) testability implementation techniques. This text

addresses testing problems and solutions arising from the size and complexity of modern semiconductor memory chips. It includes discussion of: memory fault models; test objectives; testing algorithms; hardware approaches for minimizing test time; and reliability testing and prediction. Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages. Cogently addressing the future of signal integrity and the effect it will have on the data transmission industry as a whole, this all-inclusive guide addresses a wide array of technologies, from traditional digital data transmission to microwave measurements, and accessibly examines the gap between the two. Focusing on real world applications and providing a wide array of case studies that show how each technology can be used—from backplane design challenges to advanced error correction techniques—this guide addresses many of today’s high-speed technologies while also providing excellent insight into their future direction. With numerous valuable lessons pertaining to the signal integrity industry, this resource is the ultimate must-read guide for any specialist in the design engineering field. The relentless scaling of semiconductor devices and high integration levels have lead to a steady increase in the cost of manufacturing test for integrated circuits (ICs). The higher test cost leads to an increase in the product cost of ICs. Product cost is a major driver in the consumer electronics market, which is characterized by low profit margins and the use of a variety of core-based system-on-chip (SoC) designs. Packaging has also been recognized as a significant contributor to the product cost for SoCs. Packaging cost and the test cost for packaged chips can be reduced significantly by the use of effective test methods at the wafer level, also referred to as wafer sort. Test application time is a major practical constraint for wafer sort, even more than for package test. Therefore, not all the scan-based digital test patterns can be applied to the die under test. This thesis first presents a test-length selection technique for wafer-level testing of core-based SoCs. This optimization technique, which is based on a combination of statistical yield modeling and integer linear programming (ILP), provides the pattern count for each embedded core during wafer sort such that the probability of screening defective dies is maximized for a given upper limit on the SoC test time. A large number of wafer-probe contacts can potentially lead to higher yield loss during wafer sort. An optimization framework is therefore presented to address test access mechanism (TAM) optimization and test-length selection for wafer-level testing, when constraints are placed on the number of number of chip pins that can be contacted. Next, a correlation-based signature analysis technique is presented for mixed-signal test at the wafer-level using low-cost digital testers. The proposed method overcomes the limitations of measurement inaccuracies at the wafer-level. A generic cost model is developed to evaluate the effectiveness of wafer-level testing of analog and digital cores in a mixed-signal SoC, and to study its impact on test escapes, yield loss and packaging cost. Results are presented for a typical mixed-signal "big-D/small-A" SoC from industry, which contains a large section of flattened digital logic and several large mixed-signal cores. Wafer-level test during burn-in (WLTBI) is an emerging practice in the semiconductor industry that allows testing to be performed simultaneously with burn-in at the wafer-level. However, the testing of multiple cores of a SoC in parallel during WLTBI leads to constantly-varying device power during the duration of the test. This power variation adversely affects predictions of temperature and the time required for burn-in. A test-scheduling technique is presented for WLTBI of core-based SoCs, where the primary objective is to minimize the variation in power consumption during test. A secondary objective is to minimize the test application time. Finally, this thesis presents a test-pattern ordering technique for WLTBI. The objective here is to minimize the variation in power consumption during test application. The test-pattern ordering problem for WLTBI is solved using ILP and efficient heuristic techniques. The thesis also demonstrates how test-pattern manipulation and pattern-ordering can be combined for WLTBI. Test-pattern manipulation is carried out by carefully filling the don't-care (X) bits in test cubes. The X-fill problem is formulated and solved using an efficient polynomial-time algorithm. In summary, this research is targeted at cost-efficient wafer-level test and burn-in of current- and next-generation semiconductor devices. The proposed techniques are expected to bridge the gap between wafer sort and package test, by providing cost-effective wafer-scale test solutions. The results of this research will lead to higher shipped-product quality, lower product cost, and pave the way for known good die (KGD) devices, especially for emerging technologies such as three-dimensional integrated circuits. Plunkett's InfoTech Industry Almanac presents a complete analysis of the technology business, including the convergence of hardware, software, entertainment and telecommunications. This market research tool includes our analysis of the major trends affecting the industry, from the rebound of the global PC and server market, to consumer and enterprise software, to super computers, open systems such as Linux, web services and network equipment. In addition, we provide major statistical tables covering the industry, from computer sector revenues to broadband subscribers to semiconductor industry production. No other source provides this book's easy-to-understand comparisons of growth, expenditures, technologies, imports/exports, corporations, research and other vital subjects. The corporate profile section provides in-depth, one-page profiles on each of the top 500 InfoTech companies. We have used our massive databases to provide you with unique, objective analysis of the largest and most exciting companies in: Computer Hardware, Computer Software, Internet Services, E-Commerce, Networking, Semiconductors, Memory, Storage,

Information Management and Data Processing. We've been working harder than ever to gather data on all the latest trends in information technology. Our research effort includes an exhaustive study of new technologies and discussions with experts at dozens of innovative tech companies. Purchasers of the printed book or PDF version may receive a free CD-ROM database of the corporate profiles, enabling export of vital corporate data for mail merge and other uses. Microelectronic packaging has been recognized as an important "enabler" for the solid state revolution in electronics which we have witnessed in the last third of the twentieth century. Packaging has provided the necessary external wiring and interconnection capability for transistors and integrated circuits while they have gone through their own spectacular revolution from discrete device to gigascale integration. At IBM we are proud to have created the initial, simple concept of flip chip with solder bump connections at a time when a better way was needed to boost the reliability and improve the manufacturability of semiconductors. The basic design which was chosen for SLT (Solid Logic Technology) in the 1960s was easily extended to integrated circuits in the '70s and VLSI in the '80s and '90s. Three I/O bumps have grown to 3000 with even more anticipated for the future. The package families have evolved from thick-film (SLT) to thin-film (metallized ceramic) to co-fired multi-layer ceramic. A later family or ceramics with matching expansivity to sili con and copper internal wiring was developed as a predecessor of the chip interconnection revolution in copper, multilevel, submicron wiring. Powerful server packages have been de veloped in which the combined chip and package copper wiring exceeds a kilometer. All of this was achieved with the constant objective of minimizing circuit delays through short, efficient interconnects. Electrostatic discharge (ESD) continues to impact semiconductormanufacturing, semiconductor components and systems, astechnologies scale from micro- to nano electronics. This bookintroduces the fundamentals of ESD, electrical overstress (EOS),electromagnetic interference (EMI), electromagnetic compatibility(EMC), and latchup, as well as provides a coherent overview of thesemiconductor manufacturing environment and the final systemassembly. It provides an illuminating look into the integration ofESD protection networks followed by examples in specifictechnologies, circuits, and chips. The text is unique in covering semiconductor chip manufacturingissues, ESD semiconductor chip design, and system problemsconfronted today as well as the future of ESD phenomena andnano-technology. Look inside for extensive coverage on: The fundamentals of electrostatics, triboelectric charging, andhow they relate to present day manufacturing environments ofmicro-electronics to nano-technology Semiconductor manufacturing handling and auditing processing toavoid ESD failures ESD, EOS, EMI, EMC, and latchup semiconductor component andsystem level testing to demonstrate product resilience from humanbody model (HBM), transmission line pulse (TLP), charged devicemodel (CDM), human metal model (HMM), cable discharge events (CDE),to system level IEC 61000-4-2 tests ESD on-chip design and process manufacturing practices andsolutions to improve ESD semiconductor chip solutions, alsopractical off-chip ESD protection and system level solutions toprovide more robust systems System level concerns in servers, laptops, disk drives, cellphones, digital cameras, hand held devices, automobiles, and spaceapplications Examples of ESD design for state-of-the-art technologies,including CMOS, BiCMOS, SOI, bipolar technology, high voltage CMOS(HVCMOS), RF CMOS, smart power, magnetic recording technology,micro-machines (MEMs) to nano-structures ESD Basics: From Semiconductor Manufacturing to ProductUse complements the author’s series of books on ESDprotection. For those new to the field, it is an essentialreference and a useful insight into the issues that confront moderntechnology as we enter the Nano-electronic Era. Global Best Practice in Private Equity Investing Private Equity in Action takes you on a tour of the private equity investment world through a series of case studies written by INSEAD faculty and taught at the world's leading business schools. The book is an ideal complement to Mastering Private Equity and allows readers to apply core concepts to investment targets and portfolio companies in real-life settings. The 19 cases illustrate the managerial challenges and risk-reward dynamics common to private equity investment. The case studies in this book cover the full spectrum of private equity strategies, including: Carve-outs in the US semiconductor industry (LBO) Venture investing in the Indian wine industry (VC) Investing in SMEs in the Middle East Turnaround situations in both emerging and developed markets Written with leading private equity firms and their advisors and rigorously tested in INSEAD's MBA, EMBA and executive education programmes, each case makes for a compelling read. As one of the world's leading graduate business schools, INSEAD offers a global educational experience. The cases in this volume leverage its international reach, network and connections, particularly in emerging markets. Private Equity in Action is the companion to Mastering Private Equity: Transformation via Venture Capital, Minority Investments & Buyouts, a reference for students, investors, finance professionals and business owners looking to engage with private equity firms. From deal sourcing to exit, LBOs to responsible investing, operational value creation to risk management, Mastering Private Equity systematically covers all facets of the private equity life cycle. This book describes efficient techniques for production testing as well as for periodic maintenance testing (specifically in terms of multi-cell faults) in modern semiconductor memory. The author discusses background selection and address reordering algorithms in multi-run transparent march testing processes. Formal methods for multi-run test generation and many solutions to increase their efficiency are described in detail. All methods presented ideas are verified by both

analytical investigations and numerical simulations. Provides the first book related exclusively to the problem of multi-cell fault detection by multi-run tests in memory testing process; Presents practical algorithms for design and implementation of efficient multi-run tests; Demonstrates methods verified by analytical and experimental investigations. Wafer-level testing refers to a critical process of subjecting integrated circuits and semiconductor devices to electrical testing while they are still in wafer form. Burn-in is a temperature/bias reliability stress test used in detecting and screening out potential early life device failures. This hands-on resource provides a comprehensive analysis of these methods, showing how wafer-level testing during burn-in (WLTBI) helps lower product cost in semiconductor manufacturing. Engineers learn how to implement the testing of integrated circuits at the wafer-level under various resource constraints. Moreover, this unique book helps practitioners address the issue of enabling next generation products with previous generation testers. Practitioners also find expert insights on current industry trends in WLTBI test solutions. Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages. SEOUL Magazine is a travel and culture monthly designed to help both expats and tourists get the most of their stay in the city, whether they're in for only a few days or dedicated lifers who are always in search of new places, facts and interesting events. Featuring in-depth reporting on how to enjoy the city, foreigners' perspectives on life as an expat in Korea and more, SEOUL is an eclectic publication that has something for everyone, whether you're looking for an interesting read or a simple source of information. Providing a complete introduction to the state-of-the-art in high-speed digital testing with automated test equipment (ATE), this practical resource is the first book focus exclusively on this increasingly important topic. Featuring clear examples, this one-stop reference covers all critical aspects of the subject, from high-speed digital basics, ATE instrumentation for digital applications, and test and measurements, to production testing, support instrumentation and text fixture design. This in-depth volume also discusses at advanced ATE topics, such as multiplexing of ATE pin channels and testing of high-speed bi-directional interfaces with fly-by approaches. This book constitutes the refereed proceedings of the 5th International Symposium on Security in Computing and Communications, SSCC 2017, held in Manipal, India, in September 2017. The 21 revised full papers presented together with 13 short papers were carefully reviewed and selected from 84 submissions. The papers focus on topics such as cryptosystems, algorithms, primitives; security and privacy in networked systems; system and network security; steganography, visual cryptography, image forensics; applications security. This book provides a comprehensive discussion of automatic testing, diagnosis and tuning of analogue, mixed-signal and RF integrated circuits, and systems in a single source. As well as fundamental concepts and techniques, the book reports systematically the state of the arts and future research directions of those areas. A complete range of circuit components are covered and test issues from the SoC perspective. An essential reference for researchers and engineers in mixed signal testing, postgraduate and senior undergraduate students. Electronic Devices Multiple Choice Questions and Answers (MCQs): Quiz & Practice Tests with Answer Key PDF (Electronic Devices Question Bank & Quick Study Guide) includes revision guide for problem solving with hundreds of solved MCQs. "Electronic Devices MCQ" book with answers PDF covers basic concepts, analytical and practical assessment tests. "Electronic Devices MCQ" PDF book helps to practice test questions from exam prep notes. Electronic devices quick study guide includes revision guide with verbal, quantitative, and analytical past papers, solved MCQs. Electronic Devices Multiple Choice Questions and Answers (MCQs) PDF download, a book covers solved quiz questions and answers on chapters: Bipolar junction transistors, BJT amplifiers, diode applications, FET amplifiers, field effect transistors, oscillators, programmable analog arrays, semiconductor basics, special purpose diodes, transistor bias circuits, types and characteristics of diodes tests for college and university revision guide. Electronic Devices Quiz Questions and Answers PDF download with free sample book covers beginner's solved questions, textbook's study notes to practice tests. Electronics MCQs book includes high school question papers to review practice tests for exams. "Electronic Devices Quiz" PDF book, a quick study guide with textbook chapters' tests for NEET/Jobs/Entry Level competitive exam. "Electronic Devices Question Bank" PDF covers problem solving exam tests from electronics engineering textbook and practical book's chapters as: Chapter 1: Bipolar Junction Transistors MCQs Chapter 2: BJT Amplifiers MCQs Chapter 3: Diode Applications MCQs Chapter 4: FET Amplifiers MCQs Chapter 5: Field Effect Transistors MCQs Chapter 6: Oscillators MCQs Chapter 7: Programmable Analog Arrays MCQs Chapter 8: Semiconductor Basics MCQs Chapter 9: Special Purpose Diodes MCQs Chapter 10: Transistor Bias Circuits MCQs Chapter 11: Types and Characteristics of Diodes MCQs Practice "Bipolar Junction Transistors MCQ" PDF book with answers, test 1 to solve MCQ questions: Transistor characteristics and parameters, transistor structure, collector characteristic curve, derating power, maximum transistors rating, transistor as an amplifier, and transistor as switch. Practice "BJT Amplifiers MCQ" PDF book with answers, test 2 to solve MCQ questions: Amplifier operation, common base amplifier, common collector amplifier, common emitter amplifier, multistage amplifiers circuit, multistage amplifiers theory, and transistor AC equivalent circuits. Practice "Diode Applications MCQ" PDF book with answers, test 3 to solve MCQ questions: Diode limiting and clamping circuits, bridge rectifier, center tapped full wave

rectifier, electronic devices and circuit theory, electronic devices and circuits, electronics engineering: electronic devices, full wave rectifier circuit, full wave rectifier working and characteristics, integrated circuit voltage regulator, percentage regulation, power supplies, filter circuits, power supply filters, full wave rectifier, transformer in half wave rectifier, and voltage multipliers. Practice "FET Amplifiers MCQ" PDF book with answers, test 4 to solve MCQ questions: FET amplification, common drain amplifier, common gate amplifier, and common source amplifier. Practice "Field Effect Transistors MCQ" PDF book with answers, test 5 to solve MCQ questions: Introduction to FETs, JFET characteristics, JFET biasing, JFET characteristics and parameters, junction gate field effect transistor, metal oxide semiconductor field effect transistor, MOSFET biasing, MOSFET characteristics, and parameters. Practice "Oscillators MCQ" PDF book with answers, test 6 to solve MCQ questions: Oscillators with LC feedback circuits, oscillators with RC feedback circuits, 555 timer as oscillator, feedback oscillator principles, introduction of 555 timer, introduction to oscillators, LC feedback circuits and oscillators, RC feedback circuits and oscillators, and relaxation oscillators. Practice "Programmable Analog Arrays MCQ" PDF book with answers, test 7 to solve MCQ questions: Capacitor bank FPAA, FPAA programming, specific FPAAs, field programmable analog array, and switched capacitor circuits. Practice "Semiconductor Basics MCQ" PDF book with answers, test 8 to solve MCQ questions: Types of semiconductors, conduction in semiconductors, n-type and p-type semiconductors, atomic structure, calculation of electrons, charge mobility, covalent bond, energy bands, energy gap, Hall Effect, and intrinsic concentration. Practice "Special Purpose Diodes MCQ" PDF book with answers, test 9 to solve MCQ questions: Laser diode, optical diodes, pin diode, Schottky diodes, current regulator diodes, photodiode, step recovery diode, temperature coefficient, tunnel diode, varactor diodes, Zener diode applications, Zener diode: basic operation and applications, Zener equivalent circuit, Zener power dissipation, and derating. Practice "Transistor Bias Circuits MCQ" PDF book with answers, test 10 to solve MCQ questions: Bias methods, DC operating points, and voltage divider bias. Practice "Types and Characteristics of Diodes MCQ" PDF book with answers, test 11 to solve MCQ questions: Biasing a diode, characteristics curves, diode models, introduction to diodes, testing a diode, typical diodes, and voltage characteristics of diode. The first edition of Silicon Germanium Materials & Devices - A Market & Technology Overview to 2006 examines the development of the silicon germanium business over a six-year period 2001 to 2006. It analyses the trends in markets, technologies and industry structure and profiles all the major players. It is specifically aimed at users and manufacturers of substrates, epiwafers, equipment and devices. The analysis includes a competitive assessment of the market of silicon germanium vs. gallium arsenide, indium phosphide vs. other forms of silicon. Silicon Germanium Materials & Devices - A Market & Technology Overview to 2006 is designed to assist with business plans, R&D and manufacturing strategies. It will be an indispensable aid for managers responsible for business development, technology assessment and market research. The report examines the rapid development of silicon germanium from an R&D curiosity to production status. An extensive treatment from materials through processes to devices and applications it encapsulates the entire silicon germanium business of today and assesses future directions. For a PDF version of the report please call Tina Enright on +44 (0) 1865 843008 for price details. Modern electronics depend on nanoscaled technologies that present new challenges in terms of testing and diagnostics. Memories are particularly prone to defects since they exploit the technology limits to get the highest density. This book is an invaluable guide to the testing and diagnostics of the latest generation of SRAM, one of the most widely applied types of memory. Classical methods for testing memory are designed to handle the so-called "static faults," but these test solutions are not sufficient for faults that are emerging in the latest Very Deep Sub-Micron (VDSM) technologies. These new fault models, referred to as "dynamic faults", are not covered by classical test solutions and require the dedicated test sequences presented in this book. Trace Analysis of Semiconductor Materials is a guidebook concerned with procedures of ultra-trace analysis. This book discusses six distinct techniques of trace analysis. These techniques are the most common and can be applied to various problems compared to other methods. Each of the four chapters basically includes an introduction to the principles and general statements. The theoretical basis for the technique involved is then briefly discussed. Practical applications of the techniques and the different instrumentations are explained. Then, the applications to trace analysis as pertaining to semiconductor materials are discussed. Chapter 1 discusses radiochemical practice, the analysis of semiconductor materials, separation techniques, several qualitative radiochemical schemes, radiochemical purification procedures, and several earlier reported studies. Chapter 2 covers emission spectroscopy, including its potential for future applications. Discussions in Chapter 3 explain the benefits of each of the four mass spectrometric methods, namely, the isotope dilution method, complete thermal vaporization, vacuum spark technique, and the ion bombardment method. Chapter 4 focuses on the absorption, fluorescence, and polarographic methods used in general trace analysis, including examples of semiconductor material applications and other problems that result when certain impurities are introduced into the test sample. This monograph will be useful for researchers in ultra-trace analysis, nuclear physics, and analytical chemistry. Managing the power consumption of circuits and systems is now considered one of the most important challenges for the semiconductor industry. Elaborate power management

strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices. This book provides readers with an insightful guide to the design, testing and optimization of 2.5D integrated circuits. The authors describe a set of design-for-test methods to address various challenges posed by the new generation of 2.5D ICs, including pre-bond testing of the silicon interposer, at-speed interconnect testing, built-in self-test architecture, extest scheduling, and a programmable method for low-power scan shift in SoC dies. This book covers many testing techniques that have already been used in mainstream semiconductor companies. Readers will benefit from an in-depth look at test-technology solutions that are needed to make 2.5D ICs a reality and commercially viable. "Papers presented at the First International Symposium on Science and Technology of Dielectrics in Emerging Fields, held from 27th April to 2nd May, 2003 in Paris, France"--Pref.